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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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VEDDER PRICE KAUFMAN & KAMMHOLZ 222 N. LASALLE STREET CHICAGO, IL 60601			CHEN, TSE W	
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			2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/768,783

Applicant(s)

LEE, CHANG-HWA

Examiner

Tse Chen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer et al, US Publication 20040103272, hereinafter Zimmer, in view of Polyudov, US Publication 20040186988, hereinafter Polyudov.

3. In re claim 1, Zimmer discloses a method for basic input output system loading for a personal computer [fig.2] [0011-12], the method comprising:

- Prior to the availability of system memory, storing data in a cache memory [18] disposed in a central processing unit [10] [0012, 0016, 0021].
- Executing a memory initialization and sizing operation [resource balancing] using the data in the cache memory [0019, 0021, 0023].

4. Zimmer did not disclose the well-known multi-processor environment [i.e., another processor operatively coupled to the central processing unit].

5. Polyudov discloses a method wherein the start-up operation is performed by another processor [main processor] operatively coupled to the central processing unit [other processors] [0020].

6. It would have been obvious to one of ordinary skill in the art, having the teachings of Polyudov and Zimmer before him at the time the invention was made, to modify the teachings of

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Zimmer to include the teachings of Polyudov, as multi-processor environments are very well known and suitable for use in the system of Zimmer [e.g., Polyudov: 0029-30; main boot processor boots with updated information stored in another processor's cache at another node by communicating directly with the other processor via IPI instead of the inaccessible flash memory]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase processing efficiency by task dividing [Polyudov: 0020].

7. As per claim 2, Zimmer discloses, wherein storing data in the cache memory is done prior to a power on self-test operation [bist] [0021; bist stored with data before any operation].

8. As per claim 3, Zimmer discloses, wherein the cache memory is a level one cache [0012; used a primary memory].

9. As per claim 4, Zimmer discloses, wherein the cache memory is a level two cache [0020; used with main memory].

10. As per claim 7, Polyudov discloses a method wherein the start-up operation is performed by a graphics processor [main processor] operatively coupled to the central processing unit [other processors] [0020].

11. As per claim 8, Polyudov discloses, wherein the graphics processor is disposed within a chipset [0020].

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer and Polyudov as applied to claim 1 above, and further in view of Lo et al., US Patent 4922451, hereinafter Lo.

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13. Zimmer and Polyudov taught each and every limitation of the claim as discussed above.

Zimmer and Polyudov did not disclose explicitly that the start-up operation includes a memory sizing operation.

14. Lo discloses a method wherein the start-up operation includes a memory sizing operation [col.4, ll.5-8].

15. It would have been obvious to one of ordinary skill in the art, having the teachings of Lo, Zimmer and Polyudov before him at the time the invention was made, to incorporate the memory sizing operation taught by Lo to the startup operation of Zimmer and Polyudov, as the memory sizing operation is very well known in the art and suitable for use in the startup operation of Zimmer and Polyudov. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to determine the actual sizing of memory [Lo: col.4, ll.5-8], necessary for effective functioning of the computer system.

16. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer and Polyudov as applied to claim 1 above, and further in view of Gammel et al., US Publication 20030005314, hereinafter Gammel.

17. Zimmer and Polyudov taught each and every limitation of the claim as discussed above. Zimmer and Polyudov did not discuss the details associated with passing control of the cache memory.

18. Gammel discloses a method wherein a step of passing control of the cache memory includes flushing the cache memory and re-initialize the cache memory [0045; passing of control from initialization to operating system changes programs].

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19. It would have been obvious to one of ordinary skill in the art, having the teachings of Gammel, Zimmer and Polyudov before him at the time the invention was made, to modify the teachings of Zimmer and Polyudov to include the teachings of Gammel, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better secure stored data [Gammel: 0045].

20. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polyudov in view of Zimmer.

21. In re claim 9, Polyudov discloses an apparatus [fig. 1] for basic input output system loading [0002], the apparatus comprising:

- A graphics processor [54] having a start-up operation [bootable] [0026].
- A central processing unit [other processors of 2] having a memory [associated flash] [0026].
- The graphics processor writing data to the memory prior to the start-up operation [0026; writes to flash prior to starting the processors with updates].

22. Polyudov did not disclose explicitly the central processing unit having a cache memory.

23. Zimmer discloses an apparatus [fig. 2] for basic input output system loading [0011-12], the apparatus comprising a central processing unit [10] having a cache memory [14] [fig. 1] and writing data to the cache memory prior to the start-up operation [0012, 0016, 0021].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Polyudov and Zimmer before him at the time the invention was made, to modify the central processing unit taught by Polyudov to include the cache teachings of Zimmer, in order to obtain the central processing unit having a cache memory and associated operations. One of ordinary

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skill in the art would have been motivated to make such a combination as it provides a way to save die space and improve processing capabilities during early initialization [Zimmer: 0005-6, 0021].

25. As per claim 10, Zimmer discloses, wherein the start-up operation performed by the graphics processor includes a power on self test operation [bist] [0019].

26. As per claim 11, Polyudov discloses, wherein the start-up operation performed by the graphics processor includes a memory sizing operation [0033].

27. As per claim 12, Zimmer discloses, wherein the cache memory is a level one cache [0012; used a primary memory].

28. As per claim 13, Zimmer discloses, wherein the cache memory is a level two cache [0020; used with main memory].

29. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer and Polyudov as applied to claim 9 above, and further in view of Gammel.

30. Zimmer and Polyudov taught each and every limitation of the claim as discussed above. Zimmer and Polyudov disclose, wherein the graphics processor flushes the data from the cache memory [copies the data to system memory] [Zimmer: 0020]. Zimmer and Polyudov did not disclose reinitializing the cache memory.

31. In re claim 14, Gammel discloses a method comprising re-initialize the cache memory [0045; passing of control from initialization to operating system changes programs].

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Gammel, Polyudov, and Zimmer before him at the time the invention was made, to modify the teachings of Zimmer and Polyudov to include the teachings of Gammel, in order to obtain the

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claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better secure stored data [Gammel: 0045].

33. As to claim 15, Zimmer discloses, wherein the central processing unit thereupon utilizes the cache memory [0020; general purpose use].

34. As to claim 16, Polyudov discloses, wherein the graphics processor is disposed within a chipset [0020].

35. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer in view of Polyudov and Gammel.

36. In re claim 17, Zimmer discloses a method for basic input output system loading in a graphics processor [10] [fig.2 processes graphics data as is well known in the art] [0011-12], the method comprising:

- Prior to the execution of an operating system, storing data in a cache memory [18] disposed in a central processing unit [10] [0012, 0016, 0021].
- Establishing a stack assignment within the cache memory [0021, 0024].
- Executing a plurality of executable instructions using the cache memory [0019].
- Upon execution of the executable instructions, passing control of the cache memory to the operating system [0011-12, 0019; passing control to finish booting which comprises the operating system as is well known in the art].

37. Zimmer did not discuss did not disclose the well-known multi-processor environment [i.e., another processor operatively coupled to the central processing unit] and the details associated with operations of the cache memory.

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38. Polyudov discloses a method wherein the start-up operation is performed by another processor [main processor] operatively coupled to the central processing unit [other processors] [0020].

39. Gammel discloses a method comprising flushing the cache memory and re-initialize the cache memory [0045; passing of control from initialization to operating system changes programs].

40. It would have been obvious to one of ordinary skill in the art, having the teachings of Gammel, Polyudov and Zimmer before him at the time the invention was made, to modify the teachings of Zimmer to include the teachings of Polyudov and Gammel, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase processing efficiency by task dividing [Polyudov: 0020] and to better secure stored data [Gammel: 0045].

41. As per claim 18, Zimmer discloses, wherein the executable instructions include a power on self test operation [bist] [0019].

42. As per claim 19, Zimmer discloses, wherein the executable instruction are performed by a graphics processing unit [10 processes graphics data as is well known in the art].

43. As per claim 20, Zimmer discloses, wherein the cache memory is a level one cache [0012; used a primary memory].

44. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Polyudov in view of Zimmer.

45. Polyudov discloses a method for basic input output system loading [0002] comprising:

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- Storing data in a memory [flash] associated with a first processor [e.g., non-boot processors] [0020].
- Executing a memory initialization and sizing operation [data organized into tables] using the data in the cache memory [0025] using a second processor [boot processor] operatively coupled to the first processor [0020; boot processor accesses bios and associated startup data stored in flash associated with first processor].

46. Polyudov did not disclose explicitly the central processing unit having a cache memory.

47. Zimmer discloses a method for basic input output system loading for a personal computer [fig.2] [0011-12] comprising:

- Prior to the availability of system memory, storing data in a cache memory [18] disposed in a central processing unit [10] [0012, 0016, 0021].

48. It would have been obvious to one of ordinary skill in the art, having the teachings of Polyudov and Zimmer before him at the time the invention was made, to modify the central processing unit taught by Polyudov to include the cache teachings of Zimmer, as cache memories disposed in a processor are well known and suitable for use in the multi-processor environment of Polyudov. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to save die space and improve processing capabilities during early initialization [Zimmer: 0005-6, 0021, 0030; Polyudov replaces flash with processor caches would save die space while allowing data to be stored prior to availability of system memory by processors of other nodes via IPI].

Response to Arguments

49. Applicant's arguments filed November 13, 2006 have been fully considered but they are not persuasive. Applicant primarily argues that Zimmer does not teach "using a second processor operatively coupled to the central processing unit". Examiner submits that the rejection is based on a combination of Zimmer and Polyudov, where Polyudov teaches the well-known concept of a multi-processor system with a designated boot processor that accesses the memory of another processor. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Polyudov and Zimmer before him at the time the invention was made, to modify the teachings of Zimmer to include the teachings of Polyudov, as multi-processor environments are very well known to increase processing efficiency by task dividing [Polyudov: 0020].

Conclusion

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
December 4, 2006



THUAN N. DU
PRIMARY EXAMINER